REMARKS

Concurrently with the filing of an RCE Transmittal in the above-identified application, and also concurrently with the filing of an Information Disclosure Statement therein, Applicants are further amending their claims, in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants are amending claim 1 to recite that the first insulative film is patterned after the step (b) "on a product-obtainable area and on a non-product-obtainable area of the semiconductor wafer"; and to recite an additional step (g) of removing the second insulative film on the edge of the semiconductor wafer.

In addition, Applicants are adding new claims 33-46 to the application. Of these newly added claims, claims 33, 36, 40 and 43-46 are all independent claims. Claims 33, 45 and 46 in substance are the same respectively as claims 5, 19 and 20 as previously in the application; and claims 36, 40, 43 and 44 correspond respectively to claims 14, 25, 30 and 32, respectively, as previously in the application. Note that as compared with previously considered claims 14, 25, 30 and 32, presently submitted claims 36, 40, 43 and 44 recite patterning the first insulative film on a product-obtainable area and on a non-product-obtainable area of the semiconductor wafer, and also recite removing the specified insulative or conductive film on the edge of the semiconductor wafer after the step of mechanically and chemically polishing the respective film.

With respect to product-obtainable and non-product-obtainable areas, note, for example, page 2, lines 15-24, of the Substitute Specification submitted with the Preliminary Amendment filed April 17, 2002, in the above-identified application.

As for the present claims, note, for example, Embodiment 1 on pages 12-28 of the aforementioned Substitute Specification.

Of the remaining claims in the above-identified application, please note previously considered claims 6, 7, 15, 16, 18, 26 and 27, in connection with claims 34, 35, 37-39, 41 and 42, respectively, as presently submitted.

Applicants respectfully traverse the rejection of claims 19 and 20 on prior art grounds, as set forth in Item 10 on pages 4 and 5 of the Office Action mailed May 17, 2004, in the above-identified application, as applicable to present claims 45 and 46. Specifically, it is respectfully submitted that the teachings of U.S. Patent No. 6,509,270 to Held and No. 6,683,007 to Yamasaki, et al., either alone or in combination, would have neither disclosed nor would have suggested such a fabrication method of a semiconductor integrated circuit device as in the present claims, including, inter alia, removing the first conductive film on an edge of the semiconductor wafer with a polishing means using a slurry or an abrasive wheel, and patterning the first conductive film (thereby forming wiring) after the step of removing the first conductive film with the polishing means (see claim 45); or removing the first conductive film on an edge of the semiconductor wafer with a polishing means using a slurry or an abrasive wheel, after the step of patterning the first conductive film to thereby form wirings (see claim 46).

Held provides a method in which a greater pressure may be applied to a first portion of a semiconductor topography than in a second portion of the topography, such that the first portion of the topography may be polished at a faster rate than the second portion, so as to provide a substantially planar upper surface across a topography including a region adjacent to an outer edge of the topography. This

patent discloses that the first portion may, for example, be adjacent to an outer edge of the topography, while the second portion may include the center of the topography. Note column 3, lines 30-50. This patent further discloses that the method may include a polishing step which polishes a region adjacent to the outer edge of the topography at a faster rate than a region including the center of the topography, such that the method may form a substantially planar upper surface across the entirety of the semiconductor topography. See column 3, lines 51-63.

It is respectfully submitted that Held discloses a polishing speed difference between, for example, a wafer center and a wafer edge region. It is respectfully submitted that Held does not disclose, and neither alone or in combination with the teachings of Yamasaki, et al., would have suggested, wafer edge polishing after the conductive film is formed on the wafer, and patterning the conductive film. In this regard, it is respectfully submitted that Held only discloses conductive layer polishing using a normal chemical mechanical polishing apparatus, shown in Fig. 4.

Yamasaki, et al. discloses etching and cleaning methods for removing an unnecessary or undesired material or materials from a semiconductor wafer, wherein, according to one aspect, the semiconductor wafer is rotated in a horizontal plane, the wafer having a device area and a surface peripheral area on its surface, the surface peripheral area being located outside the device area; and an etching liquid is emitted toward the surface peripheral area of the wafer by an edge nozzle, thereby selectively etching out an unnecessary material existing in the surface peripheral area. Note, e.g., column 7, lines 6-17. See also column 8, lines 1-12, describing a further method aspect (a cleaning method) of Yamasaki, et al.

It is respectfully submitted that Yamasaki, et al., either alone or in combination with the teachings of Held, would have neither taught nor would have suggested the subject matter of presently submitted claims 45 and 46, including the removal of the first conductive film on an edge of the semiconductor wafer with a polishing means and thereafter patterning the first conductive film, as in claim 45, or removing the first conductive film on the edge of the semiconductor wafer with a polishing means after patterning, as in claim 46.

The contention by the Examiner on page 5 of the Office Action mailed May 17, 2004, that Yamasaki, et al. discloses patterning of the conductive layer before the edge removal step and after the edge removal step, in columns 15 and 16 thereof, is respectfully traversed. It is respectfully submitted that Yamasaki, et al. discloses wafer edge etching after forming a copper film in the wiring trench, as shown in step S4 of Fig. 11. As shown in Fig. 12D of Yamasaki, et al., the copper film 42 is removed from the edge region for preventing a copper contamination by a delaminated copper film from the wafer edge portion. Then, the wafer edge cleaning S7 (not polishing), as seen in Fig. 11, is conducted for the residue, after a chemical mechanical polishing process, by using a same etching solution shown in Fig. 12F (note column 15, lines 7-10, and column 16, lines 23-28 and 34-49, of Yamasaki, et al.). Thus, it is respectfully submitted that Yamasaki, et al., disclosing wafer edge etching, and it is respectfully submitted that this reference, either alone or in combination with the teachings of Held, would have neither disclosed nor would have suggested the polishing as in the present claims.

Accordingly, it is respectfully submitted that the combined teachings of Held and of Yamasaki, et al. would have neither disclosed nor would have suggested the

subject matter of present claims 45 and 46, including, inter alia, the removing of the first conductive film on the edge of the wafer with a polishing means.

The following additional comments are provided in connection with the documents being concurrently submitted with the concurrently filed Information Disclosure Statement.

U.S. Patent No. 6,361,708 to Kubo, et al. discloses a removal of a tungsten metal film around a wafer edge portion. This metal removing is conducted by polishing for the upper, middle and lower surfaces of a wafer edge portion. See Figs. 6 and 7, as well as from column 6, line 55 to column 7, line 19, of Kubo, et al. The purpose of the wafer edge polishing is for preventing particles of tungsten film at the wafer edge from separating, and preventing the wafer from contamination by the separated particles of the tungsten film. This wafer edge polishing is conducted prior to chemical mechanical polishing of the tungsten film. It is respectfully submitted that No. 6,361,708 would have neither disclosed nor would have suggested the patterning on a product-obtainable area and on a non-product obtainable area of the semiconductor wafer, as in various of the present claims, which achieves polished planarity of the wafer surface.

United States Patent Application Publication No. US 2001/0051432 to Yano, et al. discloses a wafer edge polishing procedure. See, e.g., paragraphs [0038] and [0039] on page 3 and the embodiments on page 4-7. Yano, et al. discloses a patterning on the die-obtainable area on the wafer (note, for example, Figs. 3A-3G, 4A-4C and 5A-5F).

It is respectfully submitted that Yano, et al. would have neither disclosed nor would have suggested patterning on the non-product-obtainable area of the

semiconductor wafer in addition to on the product-obtainable areas thereof, and advantages thereof as achieved by the present invention in improving planarity.

Furthermore, it is respectfully submitted that neither of Kubo, et al. or Yano, et al. would have disclosed or would have suggested the polishing of the wafer edge after the chemical and mechanical polishing of the surface to planarize the surface thereof, as in various of the present claims.

In view of all of the foregoing, and particularly in view of the presently submitted RCE Transmittal, entry of the present amendments, and entry of record of the concurrently filed Information Disclosure Statement, and further examination of the above-identified application including in light of, inter alia, the documents submitted with the enclosed Information Disclosure Statement, are respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 501.41261X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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